

Usage and Application of μ PB1509GV 1-GHz Input Divide by 2, 4, 8 Prescaler IC for Portable Radio Systems

[MEMO]

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Precautions for design-ins

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form the ground pattern as wide as possible to minimize the ground impedance. In particular, the line connected to the ground pin should be as short as possible.
- (3) A bypass capacitor should be attached to each Vcc pin.
- (4) The DC cut capacitor must be externally attached to each signal pin.
- (5) Each input pin must not externally adjust the pin voltage.
- (6) When pull down the output pin with a DC resistor, choose a resistor with a resistance larger than 200 Ω .
- (7) Beware that if the load impedance Z_L is smaller than 200 Ω the output amplitude is too low, resulting in a low DU ratio with the second order harmonics.

This document outlines a typical application of this product, that is, provides a sample concept for designing an external circuit directly required for this product. NEC only assures the quality and characteristics of this product specified in the Data Sheet, and is not responsible for any user's product designs or application sets.

The peripheral circuit shown in this document is just an example prepared for evaluating the operations of this product, and does not imply that the circuit configurations or constants are recommended values or regulations. In addition, these circuits are not intended for any mass-produced application sets. This is because the RF characteristics vary depending on the external parts used, mounting patterns, and other conditions.

Therefore, it is the responsibility of the user to design the external circuit according to the user-desired system requirements while referring to the information in this document and to use it after confirming the characteristics on the user's application set.

The information in this document will be updated without notice.

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Reference Documents

[MEMO]

1. INTRODUCTION

In the consumer electronic appliances, the proportion of portable to stationary models has been considerably growing these days. Especially in portable radios and wireless transceivers, pocket-size appliances instead of the conventional carrying types are leading this market. What is more, due to small size and light weight, battery downsizing and lower operating voltage are needed. Based on the trend of portable appliances utilizing RF waves, the ICs in these appliances are also required to have a smaller size and a lower operating voltage.

In order to meet these requirements, NEC, which had marketed products with the part number μ PB5xx as conventional-type prescaler ICs, has recently developed and released the μ PB1509GV low-voltage shrink package prescaler IC.

This document describes the features and application examples for this IC.

2. PRODUCT OUTLINE

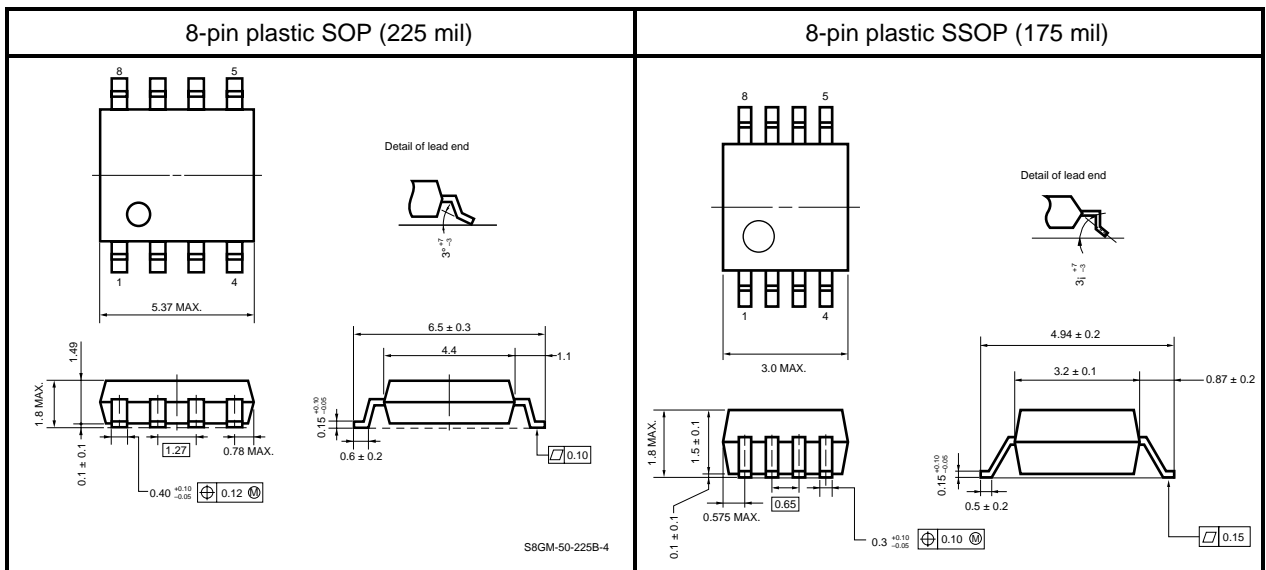
2.1 Features

The μ PB1509GV is a monolithic silicon IC designed as a prescaler for portable radio systems. This IC can be used as the front-end prescaler for the PLL frequency synthesizer incorporated in the 17K Series of DTS controllers. The greatest difference with the previous prescaler IC of μ PB587G is that the μ PB1509GV uses a shrink package to reduce the space in the application set. Although the pin pitch of this shrink package is narrower than μ PB587G, a high isolation is achieved by using the same pin configuration as for NEC's conventional products, arranging input and output pins back-to-back, and devising internal circuit designs. Table 2-1 shows the comparison of characteristics with the conventional product and Figure 2-1 compares the dimensions of these products.

Table 2-1. Characteristic Comparison with the μ PB587G

Part Number	I _{cc} (mA)	V _{cc} (V)	Divide by 2 Mode f _{in} (MHz)	Divide by 4 Mode f _{in} (MHz)	Divide by 8 Mode f _{in} (MHz)	Package	Pin Configuration
μ PB587G	5.5	2.2 to 3.5	50 to 300	50 to 600	50 to 1000	8-pin plastic SOP (225 mil)	NEC original configuration
μ PB1509GV	5.0	2.2 to 5.5	50 to 700	50 to 800	50 to 1000	8-pin plastic SSOP (175 mil)	

Figure 2-1. 8-Pin Plastic SOP (225 mil) vs. 8-Pin Plastic SSOP (175 mil)



The major features and applications of the μ PB1509GV are described below.

[Features]

- <1> Small size for space reduction : 8-pin plastic SSOP (175 mil)
Package size = $3.0 \times 3.2 \times 1.8$ mm
- <2> Low current consumption suitable to battery-driven systems : $5.0 \text{ mA}_{\text{TYP}}$ at $V_{\text{CC}} = 3.0 \text{ V}$ (4.0 mA at 2.2 V)
- <3> Wider range of power supply voltage allowing flexible designs : $V_{\text{CC}} = 2.2$ to 5.5 V
- <4> Wider range of operating frequency providing various system configuration options : $f_{\text{in}} = 50 \text{ MHz}$ to 700 MHz in divide by 2 mode
 $f_{\text{in}} = 50 \text{ MHz}$ to 800 MHz in divide by 4 mode
 $f_{\text{in}} = 50 \text{ MHz}$ to 1000 MHz in divide by 8 mode
- <5> Selectable divide ratios allowing an optimal response frequency to be specified for succeeding stages : $f_{\text{out}} = 25 \text{ MHz}$ to 350 MHz in divide by 2 mode
 $f_{\text{out}} = 12.5 \text{ MHz}$ to 200 MHz in divide by 4 mode
 $f_{\text{out}} = 6.25 \text{ MHz}$ to 125 MHz in divide by 8 mode

[Typical applications]

- Portable radios
- Portable radio communication systems

2.2 Process Technology

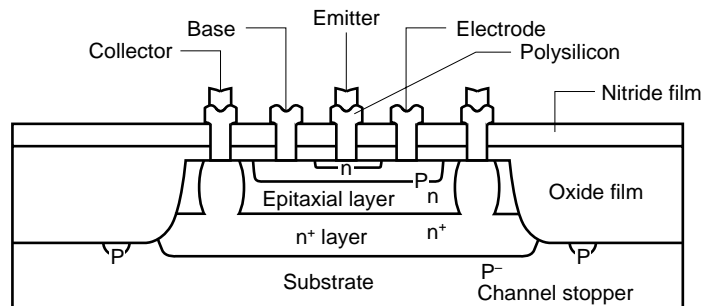
The μ PB1509GV is manufactured using NEC-proprietary silicon bipolar process technology called NESATTMIV. This section describes the features of this process.

The cross-sectional drawing of the transistor manufactured using this process is shown in Figure 2-1. The following roughly explains the major features of this process.

- <1> A high gain-bandwidth product (f_T) is realized by reduction of the emitter junction thickness of the transistor. ($f_T = 20 \text{ GHz}$ for NESATTMIV and $f_T = 10 \text{ GHz}$ for NESATTMII).
- <2> Low-noise and high-gain operation is realized due to a reduced base resistance and E-B junction capacitance by minimizing the emitter width and base junction thicknesses of the transistor (emitter width = $0.6 \mu\text{m}$ for NESATTMIV and = $1.0 \mu\text{m}$ for NESATTMII).
- <3> For high reliability such as high moisture proofness, the direct nitride-film construction process is used in which a nitride film covers the base and emitter surface previously covered by a thin oxide film.

The features of this process realize high-performance ICs having high reliability and electrical characteristics.

Figure 2-2. Cross-Sectional Drawing of Transistor (Elements in IC) using NESAT Process



2.3 Internal Circuit

Figure 2-3 shows the internal circuit configuration of the μ PB1509GV. The input stage includes an on-chip amplifier for securing high sensitivity and the output stage amplifier for maintaining a sufficient output level, which both realize a wide operation range. The frequency divider section consists of three master-slave T-type flip-flop circuits, each dividing its input frequency by two.

Each block operates as follows. Each flip-flop in the μ PB1509GV divides its input frequency at each falling edge of the input signal from the IN pin (rising edge with the μ PB587G). The first stage flip-flop (Divider 1) performs the divide by 2 operation all the time, while the other two flip-flops are enabled or disabled by the SW1 and SW2 control signals. When SW1 or SW2 is connected to the V_{CC1} line, the respective flip-flop passes on its input to the next stage; when SW1 or SW2 is connected to GND or left unconnected, it divides its input by 2 and passes on the result to the next stage, which allows users to select a frequency divide ratio from among 2, 4, and 8 according to the combination of these control signals. The amplifier of the output stage is of the emitter-follower configuration and provides a stable output level little influenced by the load impedance. For details, refer to **3.2 Load Impedance and Characteristics**.

Figure 2-3. Internal Block Diagram of μ PB1509GV

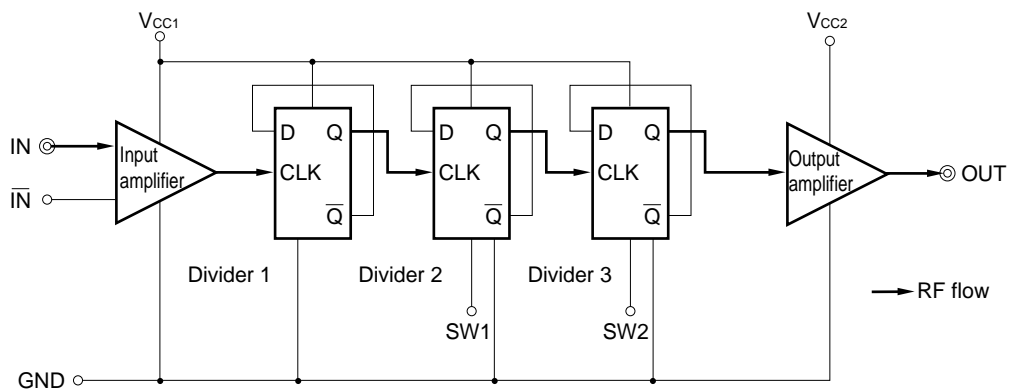
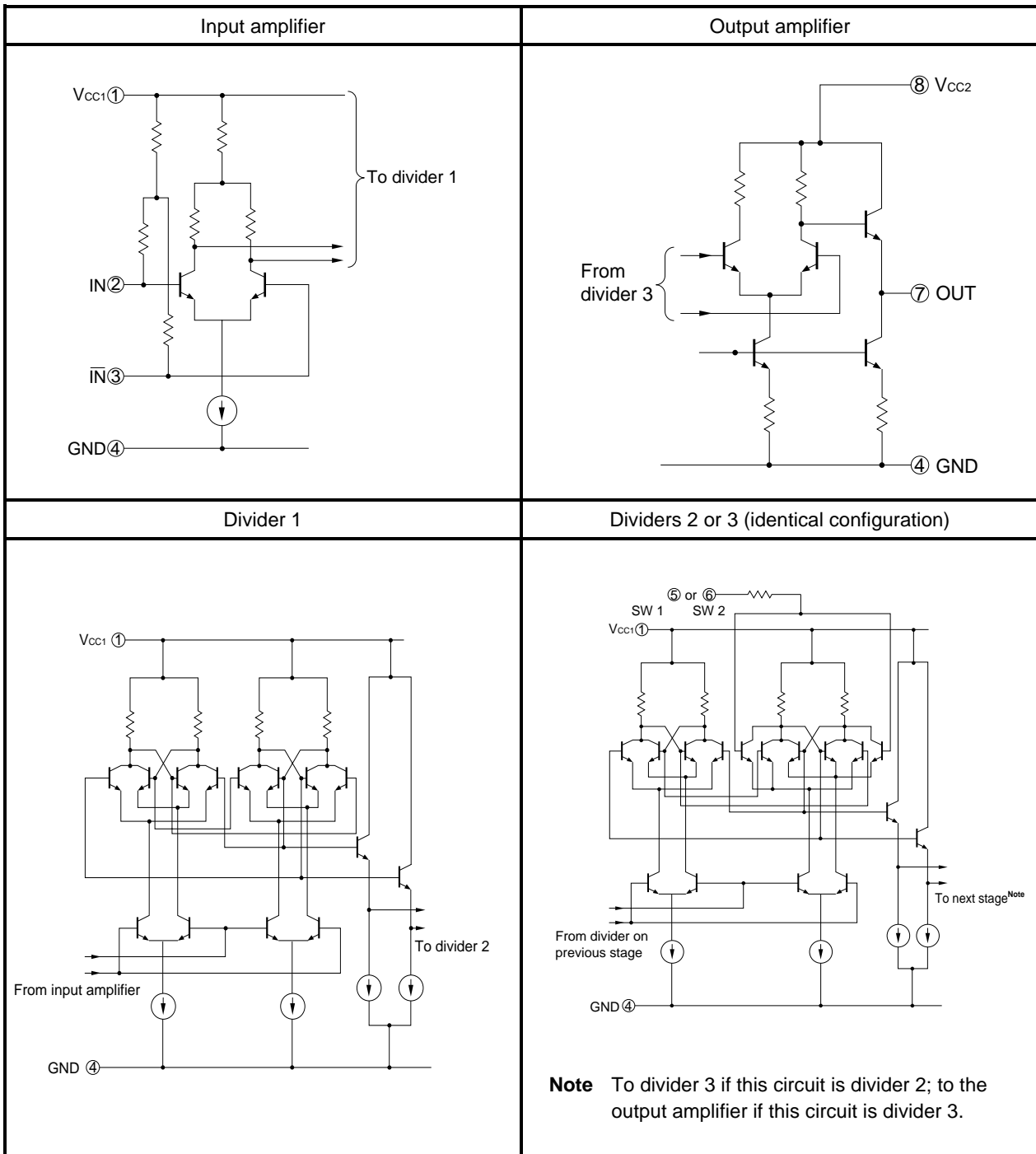


Figure 2-4. Equivalent Circuits of Prescaler's Internal Blocks



2.4 Characteristics and Measurement

(1) Input/output impedance

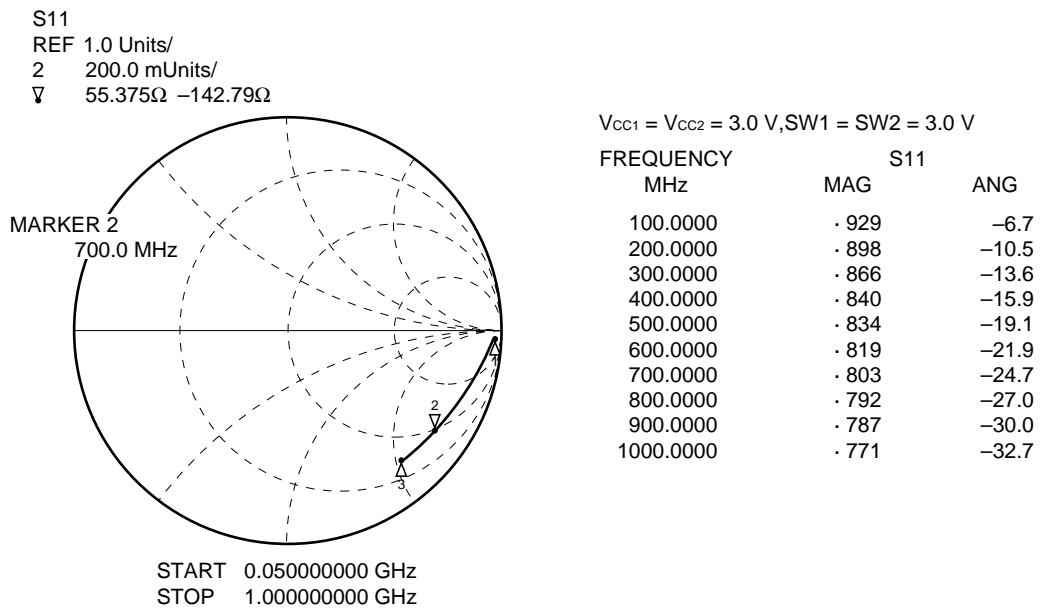
This section describes the input/output impedance characteristics. As shown in Figure 2-5 (a), the μ PB1509GV's input impedance against the mixer's LO input impedance is high enough (higher than $150\ \Omega$) and connecting a voltage-controlled oscillator (VCO) is considered to cause no problem because the load is negligible in parallel connection.

The output impedance fluctuates little and provides a stable output due to the emitter-follower circuit output configuration. As shown in Figure 2-5 (b), the output impedance is between 150 and $200\ \Omega$ and assures that the output amplitude of $0.1\ V_{P-P}$ MIN can be obtained at a load impedance of $200\ \Omega$ measured with the test circuit specified in the Data Sheet.

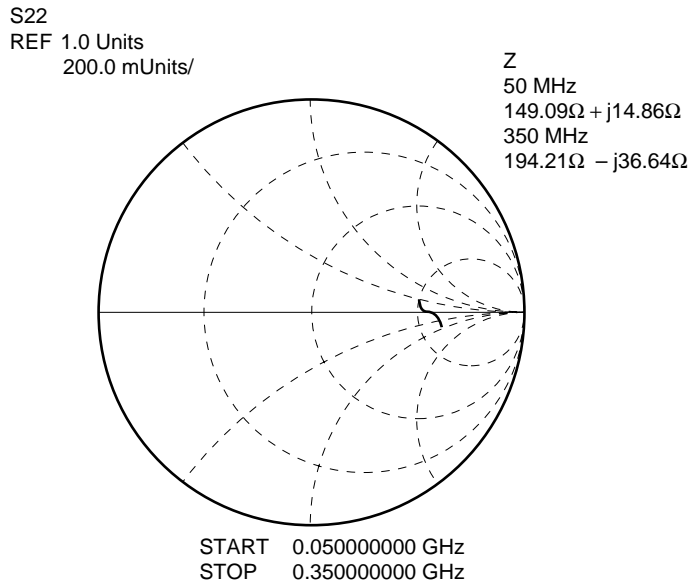
Note that the test circuit includes a $150\ \Omega$ resistor in front of the counter which is synthesized with the instrument impedance in order to alternatively create a load impedance of $200\ \Omega$. However, this resistor is for measurement purposes only and is not required in actual applications.

Figure 2-5. Smith Chart for μ PB1509GV ($V_{CC1} = V_{CC2} = 3.0\ V$, $SW1 = SW2 = 3.0\ V$)

(a) S11 (Input impedance)



(b) S22 (Output impedance)



(2) Divide ratio setting pins

Although this IC has a divide ratio selection function (2, 4, or 8), it is assumed to be used with a fixed ratio. Because of this, the divide ratio setting pins (SW1 and SW2) are designed so that they are clamped to either high or low level unlike common prescalers. The SW1 and SW2 pins in the test circuit shown below are connected to the external switches that clamp these pins high (connected to the V_{CC1} pin) or low (connected to the GND or leave OPEN). These external switches are provided to test the operations with all divide ratios. In application sets that basically do not need to operate with plural ratios, however, connect each SW pin permanently to either the V_{CC1} pin or GND pattern (or left OPEN) to fix the ratio.

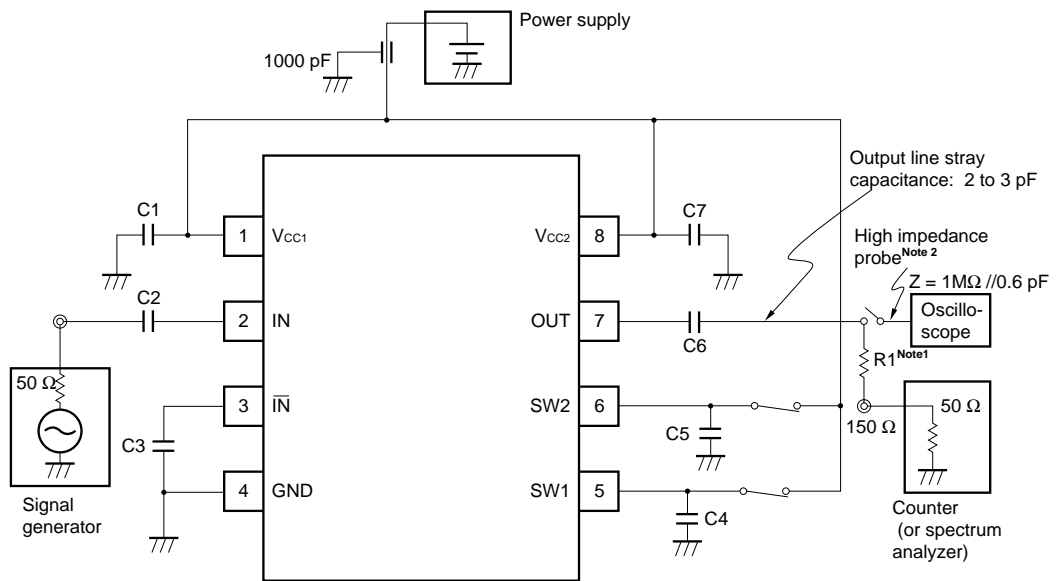
Therefore, it is recommended that the users specify a divide ratio when designing an application set. The description “H level = V_{CC} and L level = GND or OPEN” shown in the electrical specifications implies this recommendation. For your reference, the following table shows the input voltages and sink current values (design values) for the H and L levels.

Table 2-2. Design Values of Divide Ratio Setting Pins
(T_A = -40 to +85 °C, V_{CC} = 2.2 to 5.5 V, for both SW1 and SW2)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
H level input voltage (SW1, SW2)	V _{IH1,2}	V _{CC}	-	V _{CC} +0.3	V	
L level input voltage (SW1, SW2)	V _{IL1,2}	GND	-	V _{CC} -1.0	V	
H level sink current (SW1, SW2)	I _{IH1,2}	2.1	4.4	6.4	μA	When T _A = +25 °C, V _{CC} = 3.0 V
L level sink current (SW1, SW2)	I _{IL1,2}	0	0	0	A	

However, in some application circuits, an external logic such as CMOS or TTL controls the switches. In this case, refer to **3.3 External Control of Divide Ratio Setting Pins**.

Figure 2-7. Test Circuit for μ PB1509GV



Equipment

Signal Generator (HP-8665A)

A counter (HP5350B) is used to measure the input sensitivity.

(Alternatively, a spectrum analyzer can be used to monitor the output frequency.)

An oscilloscope is used to monitor the output amplitude.

(When a spectrum analyzer is used to monitor the output power, disconnect the probe of the oscilloscope.)

Divide ratios and pin connections

		SW2	
		Connected to V _{CC1} pin	Connected to GND or leave OPEN
	Connected to V _{CC1} pin	1/2	1/4
SW1	Connected to GND or leave OPEN	1/4	1/8

Parts

Type	Value
C1 to C7	1000 pF
R1	150 Ω ^{Note 1}

[Precautions on measurement]

Notes 1. In the test circuit, set R1 so that R1 + instrument impedance is 200 Ω for the measured IC. R1 is unnecessary in actual applications.

2. Use an oscilloscope connected with a high-impedance RF probe when measuring the output amplitude with the test circuit shown in the Data Sheet. If a spectrum analyzer is used to monitor the output frequency as an alternative for the counter, note that the power level displayed on the analyzer screen may be lower than the actual value because of the inserted resistor.

$$\text{On-display decrease } \Delta P \text{ (dB)} = 10 \log \frac{R1 + Z_{me}}{Z_{me}}$$

where, R1 is the RF resistance to create a pseudo load impedance for the test circuit, and Z_{me} is the instrument impedance.

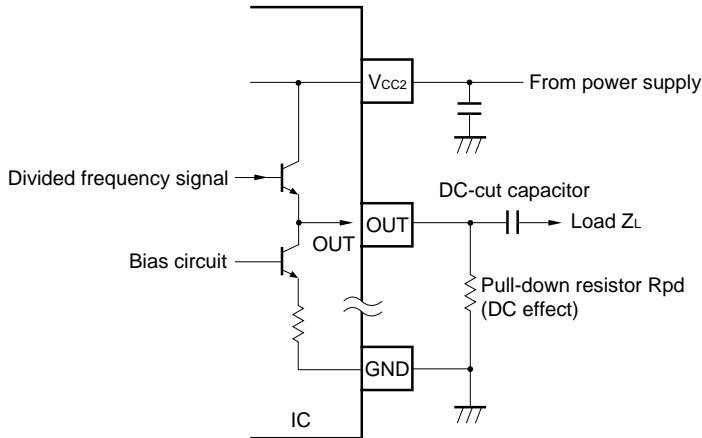
Because R1 = 150 Ω and Z_{me} = 50 Ω in the test circuit, ΔP = 6 dB.

3. APPLICATION CIRCUIT DESIGN EXAMPLES

3.1 Output Amplitude Improvement

If the output amplitude is insufficient when the load is in the high impedance state, pull down the output pin of the μ PB1509GV with a DC resistor, so that the circuit current in the internal output amplifier can be increased as a DC effect and the output amplitude can be increased. An example of an external circuit connected to the output stage is shown in Figure 3-1. V_{CC2} for the internal output amplifier is independent of V_{CC1} . In this case, calculating based on the internally allowable maximum current, use a pull-down resistor whose resistance R_{pd} is larger than 200 Ω . (Refer to the **Caution on page 10.**)

Figure 3-1. Example of External Circuit for Output Stage



$$V_{out} (V_{P-P}) = 2 \sqrt{2 \times P_o (W) \times Z_L (\Omega)}$$

If R_{pd} is not included,

At $Z_L = 200 \Omega$, since $V_{out} = 0.1 V_{P-P} \text{ MIN.}$,

$P_o = 6.25 \times 10^{-6} \text{ W MIN (= -22 dBm)}$

$$\therefore V_{out} = 7.1 \times 10^{-3} \sqrt{Z_L} V_{P-P} \text{ MIN}$$

<1> If $Z_L \geq 400 \Omega$, then the output compression will be entered.

<2> If R_{pd} is included, the underlined value increases according to the circuit current increase.

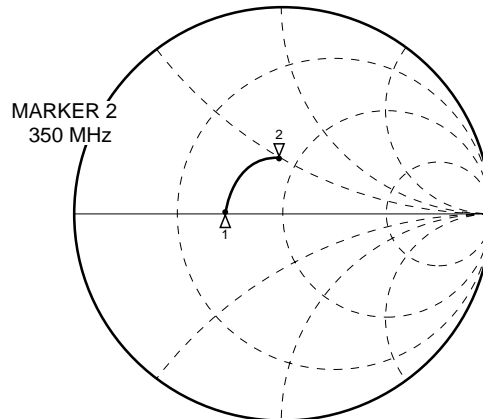
When an external DC pull-down resistor increases the current of output amplifier, the output impedance becomes 40 to 50 Ω , as shown in Figure 3-2. In this case, however, there is no change in the input impedance of the input amplifier since the current increased flows only on the output stage.

You should note that this pull-down resistor is different from the RF resistor (for load impedance) that appears in the Data Sheet.

Figure 3-2. Output Impedance Change by Output Pin's Pull-Down Resistor
($V_{CC1} = V_{CC2} = 3.0 \text{ V}$, $SW1 = SW2 = 3.0 \text{ V}$)

Pull-Down Resistor $R_{pd} = 1.2 \text{ k}\Omega$

S22 Z
REF 1.0 Units/
2 200.0 mUnits/
▽ 43.428 Ω 25.484 Ω



START 0.05000000 GHz
STOP 0.35000000 GHz

[Pull-Down Resistor on Output Pin to Increase Output Amplitude]

An effective way to increase the output amplitude is to increase the circuit current of the internal output stage by connecting a DC pull-down resistor to the emitter-follower output pin. The μ PB1509GV, however based on the maximum allowable current of the internal circuits, connect a DC pull-down resistor of 200 Ω MIN to the output pin (1.2 k Ω MIN with the μ PB587G).

A supplementary explanation follows. In the case of the test circuit shown in the Data Sheet, the specification of the output amplitude is defined on the load impedance of 200 Ω . Therefore, due to the 1.2 k Ω pull-down resistor connection, the circuit current is increased by 2 mA at $V_{CC} = 3.0$ V and output amplitude by about 0.3 V_{P-P} , compared with the above-mentioned test circuit. In addition to this DC effect, the pull-down resistor has the following secondary effect: although the characteristic impedance of the output pin in the RF range is decreased, this enables to drive a high-impedance device while maintaining a large amplitude.

Therefore, in actual application sets, you should check first the output amplitude under the load condition of the application set without connecting the pull-down resistor, then adjust the increase in the circuit current with the pull-down resistor connected.

3.2 Load Impedance and Characteristics

This IC assures that the output amplitude with a load of 200 Ω is 0.1 V_{P-P} MIN. However, this means that $Z_L = 200$ Ω at output amplitude measurement is assumed, not that the recommended load impedance is 200 Ω . If a high-impedance CMOS IC is connected to the following stage, the output amplitude becomes large proportionally to the load impedance value of the connected IC, and saturates at 1 k Ω or larger. Figure 3-3 shows the load impedance dependency of output amplitude for each pull-down resistor value (Rpd), and Figure 3-4 shows the circuit current dependency of output amplitude (resulting from output pin pull-down resistor) for each load impedance value.

Figure 3-3. Output Amplitude vs. Pull-Down Resistor and Load Impedance

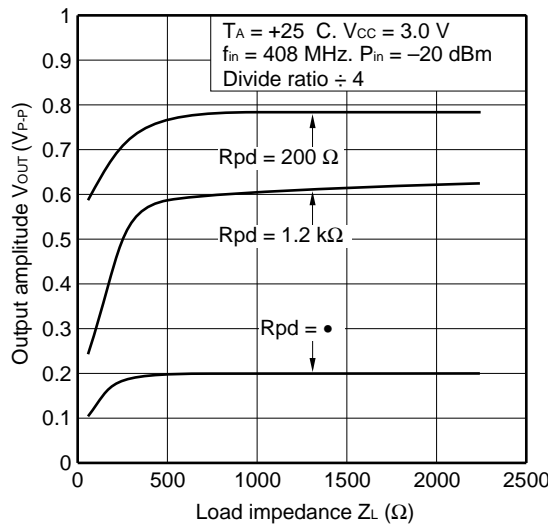
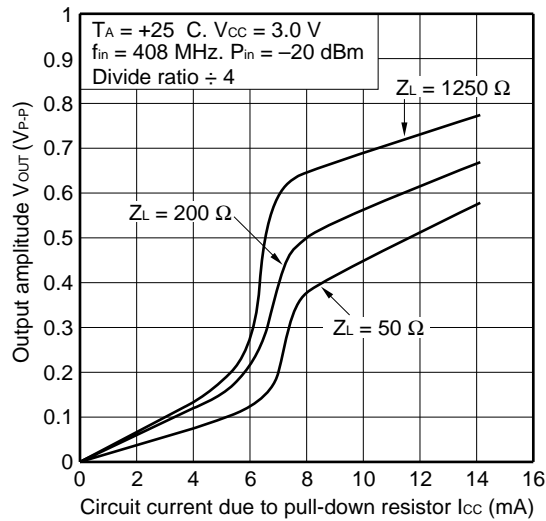


Table 3-1. Relationship between Output Amplitude and Load Impedance (Underlined values are empirical data for reference only)

Pull-Down Resistor R_{pd}	Relationship (Approximate Value in Linear Area)	I_{CC} Flowing due to Pull-Down Resistor
200 Ω	Output saturation area irrespective of Z_L	$I_{CC} = 14.1 \text{ mA}$
1.2 k Ω	$V_{out} = \underline{0.031} \sqrt{Z_L}$ (V_{P-P}) @ $Z_L < 360 \Omega$	$I_{CC} = 7.2 \text{ mA}$
∞ (without R_{pd})	$V_{out} = \underline{0.01} \sqrt{Z_L}$ (V_{P-P}) @ $Z_L < 400 \Omega$	$I_{CC} = 5.4 \text{ mA}$

Figure 3-4. Output Amplitude vs. Load Impedance and Circuit Current Dependency



Caution The external resistor on the output line works in the DC range if located closer than the DC-cut capacitor to the $\mu PB1509GV$. As in the test circuit, however, the external resistor located farther than the DC-cut capacitor works in the RF range. Note that the 150Ω external resistor R1 on the test circuit in Figure 2-7 is a test-purpose pseudo impedance element adjusting the load impedance, and is not required in actual application circuits.

3.3 External Control of Divide Ratio Setting Pins

SW1 and SW2 of this IC allow users to select a divide ratio from among 2, 4, and 8. By leaving these pins OPEN or connected to GND or V_{CC1} via the mounting pattern, and whether two internal frequency dividers are enabled or disabled, the combination of those determines a fixed divide ratio. On the other hand, some user's applications may need to switch divide ratio – from 2 to 4 and vice versa, for example – according to the input frequency changes. However, since the divide ratio of this IC is not intended to be controlled by external ratio switching logics, the low-level range of SW pins themselves is wide and the high-level range is narrow. (Refer to **Table 2-2. Design Values of Divide Ratio Setting Pins.**) Therefore, it is difficult to change the divide ratio by controlling the voltage applied to these pins from a simply connected CMOS logic because the threshold voltage of SW pins is $V_{CC} - 1.0 V$ to V_{CC} (V). To adjust this H/L threshold level, connect external resistors to the SW pins as shown in Figure 3-5 for example, where a pull-up resistor and a series resistor are externally connected. These external resistors and the internal elements together configure the switching circuit. The control voltage range with the external resistors is shown in Table 3-2.

Figure 3-5. Application Circuit Example for Divide Ratio Control Voltage Range Adjustment by Connecting External Resistors to SW Pin

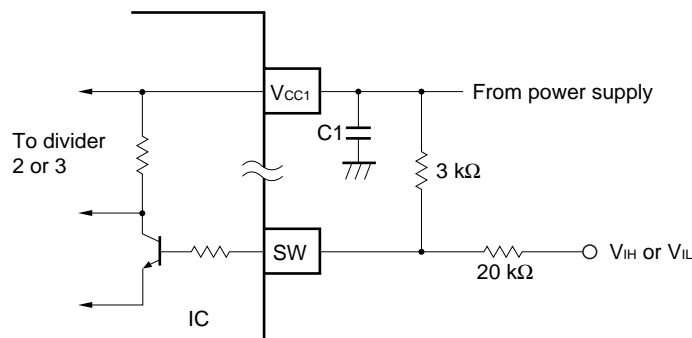


Table 3-2. Adjustment of External Control Voltage for Divide Ratio by Connecting External Resistors
 (T_A = -40 to +85 °C, V_{CC} = 2.2 to 5.5 V)

Parameter	Symbol	MIN.	MAX.	Unit
H level at O point	V _{IH}	V _{CC} - 0.2	V _{CC} + 0.5	V
L level at O point	V _{IL}	-0.2	V _{CC} × 0.4	V

4. SYSTEM EXAMPLE

4.1 Calculation of Count Number and Step Frequency for Prescaler PLL

The response frequency of the on-chip PLL frequency synthesizer (f_{synth}) in CMOS ICs such as the 17K Series is around 100 MHz even the highest. Therefore, for use in the VHF to UHF bands, the prescaler PLL method should be adopted in which the VCO oscillation frequency (f_{VCO}) of the local output is divided by a fixed-ratio prescaler before entering the frequency synthesizer. If this method is used, the count number can be expressed as follows since the system's step frequency (f_{step}) is divide-ratio times the phase comparison frequency (f_r) of the frequency synthesizer.

$$f_r = \frac{f_{step}}{P} \quad (\text{Hz})$$

P : Divide number of the prescaler

$$\frac{f_{VCO}}{P \times N} = \frac{f_{xtal}}{R} = f_r \quad (\text{Hz})$$

N : N count number of the following-stage frequency synthesizer

R : Reference count number of the following-stage frequency synthesizer

$$f_{VCO} = P \times f_{synth}$$

f_{xtal}: Reference oscillation frequency

$$\therefore \frac{f_{VCO}}{P \times N} = \frac{f_{xtal}}{R} = \frac{f_{step}}{P} = \frac{f_{synth}}{N}$$

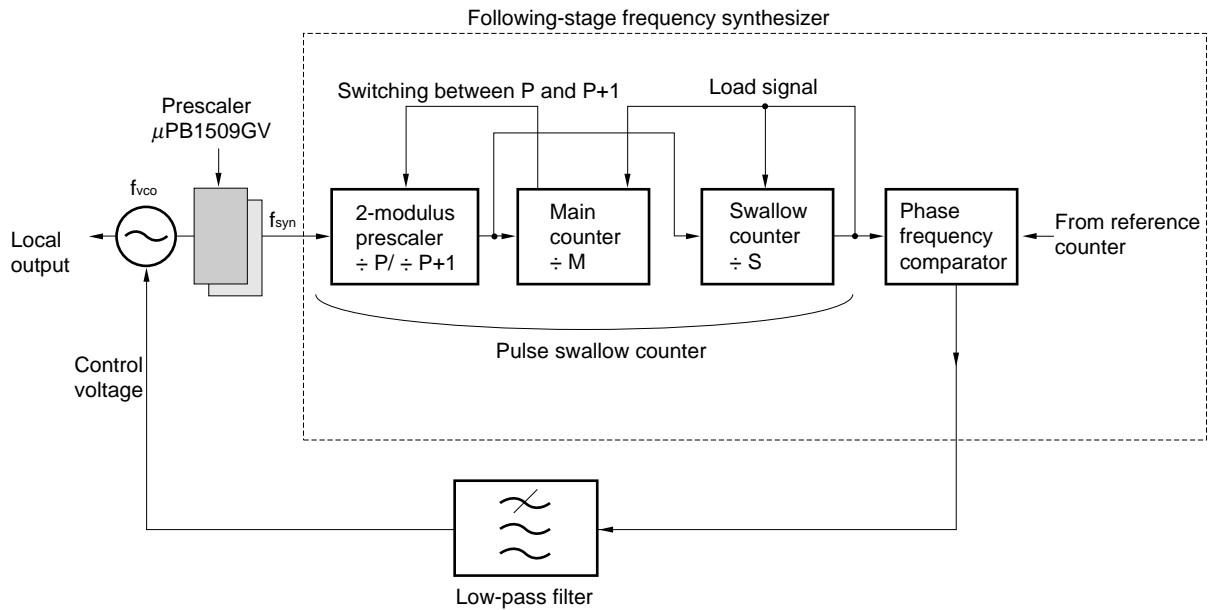
Therefore,

Relationship between divide number of the prescaler and count numbers of the following-stage frequency synthesizer (Figure 4-1 case)

$$N = \frac{f_{VCO}}{f_{step}} \dots\dots\dots N \text{ count number of prescaler side}$$

$$R = \frac{P \times f_{xtal}}{f_{step}} \dots\dots\dots \text{Reference count number of reference X'tal oscillator side}$$

Figure 4-1. Configuration in Prescaler PLL Method



Since $P = 2, 4, \text{ or } 8$, the step frequency is 2, 4, or 8 times the phase comparison frequency because the phase comparison frequency (f_r) and the step frequency (f_{step}) have the relationship: $f_{\text{step}} = P \times f_r$.

5. CONCLUSION

The above sections described the usage of the $\mu\text{PB1509GV}$ prescaler IC which is applicable for the prescaler between a local oscillator and a frequency synthesizer in portable radio systems. We believe that it is understood from this document that this IC provides a flexible design because the interface levels can be adjusted externally.

Reference documents:

- $\mu\text{PB1509GV}$ Data Sheet (Document number: P10769E)
- μPB587G Data Sheet (Document number: IC-7566A)
- Fundamentals of Frequency Synthesizer Employing PLL (Document number: P12196E)

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